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Application No.	08/936,344
Filing Date	September 24, 1997
First Named Inventor	Paul Michael Embree
Group Art Unit	2644
Examiner Name	Harvey, M.
Attorney Docket Number	80398P115

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Total Number of Pages in This Submission	16

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
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- [ ] To Convert a Provisional Application
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- [ ] Terminal Disclaimer
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- [ ] Request for Refund
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- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Additional Enclosure(s) *(please identify below):*

Appeal Brief (Original and two copies).

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Thinh V. Nguyen, Reg. No. 42,034 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	May 15, 2001

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Complete if Known	
Application No.	08/936,344
Filing Date	September 24, 1997
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☐ Applicant claims small entity status. See 37 CFR 1.27.

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

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2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	Fee Paid
Total Claims		-	=	X	=	
Independent Claims		-	=	X	=	
Multiple Dependent					=	

**or number previously paid, if greater, For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	260	204	135	Multiple Dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	*Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	*Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	390	216	195	Extension for response within second month	
117	890	217	445	Extension for response within third month	
118	1,390	218	695	Extension for response within fourth month	
128	1,890	228	945	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	310.00
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
~~169~~	~~900~~	~~169~~	~~900~~	~~Request for expedited examination~~ of a design application	
				Other fee (specify)	
				Other fee (specify)	

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 310.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Thinh V. Nguyen	Registration No. (Attorney/Agent)	42,034	Telephone	(714) 557-3800
Signature				Date	05/15/01

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#16
MDJ
5-25-01

Our Docket No.: 080398.P115

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Paul Michael Embree et al.

Application No.: 08/936,344

Filed: September 24, 1997

For: **MEMORY ALLOCATION FOR REAL-TIME AUDIO PROCESSING**

Examiner: Harvey, M.

Art Group: 2644

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231-9999

Dear Sir:

Applicants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicants also submit herewith our check number 12007 in the amount of $310.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(f). Please charge any additional fees or credit any overpayment to our deposit Account No. 02-2666.

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I. REAL PARTY IN INTEREST

The real parties in interest are the assignees, Sony Corporation and Sony Pictures Entertainment, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-15 of the present application are pending and remain rejected. The Applicants hereby appeal the rejection of claims 1-15.

IV. STATUS OF AMENDMENTS

The Applicants filed an amendment on January 19, 2001, in response to a Final Office Action issued by the Examiner on November 20, 2000. In response to the January 19, 2001, amendment, the Examiner issued an Advisory Action on February 14, 2001, denying entry of amendment. The Applicants filed a Notice of Appeal from the Advisory Action issued by the examiner on March 15, 2001.

V. SUMMARY OF INVENTION

The present invention discloses a technique to allocate memory for real-time audio processing. A system 100 includes a plurality of embedded boxes (EBX's) for processing

audio signal and audio engineering society (AES) standard input/output channels 125. Each of the EBXes includes at least one or more processors 205, a signal processing subsystem 270, and a SCSI-2 controller 250_1. [1] The signal processing system includes a memory system 300. [2] The memory system 300 includes two 2-to-1 multiplexers MUX0 310 and MUX1 311 and two dynamic random access memory (DRAM) banks BANK0 320 and BANK1 321.[3] MUX0 310 and MUX1 311 are connected to the digital signal processor (DSP) bus and the Peripheral Component Interconnect (PCI) bus and to the DRAM BANK0 320 and BANK1, respectively. The SCSI-2 controller 2501 is connected to the PCI bus. [4] Each of the MUX0 310 and MUX1 311 consists of two multiplexers: address multiplexer and data multiplexer.[5] MUX0 310 and MUX1 311 are controlled by the SEL0 and SEL1 signals, respectively. When SEL0 and SEL1 are at a first logic level, the data transfer is between the selected DRAM bank and the PCI bus to the SCSI controller 250_1. When SEL0 and SEL 1 are at a second logic level, the data transfer is between the selected DRAM bank and the DSP bus.[6] DRAM BANK0 320 and DRAM BANK1 321 are two dynamic random access memory banks operating separately and independently. [7] By controlling the SEL0 and SEL 1, the two DRAM banks can be accessed simultaneously by two different processors. For example, the SCSI controller may access the DRAM BANK0 320 for storing data while the DSP is reading the data out from DRAM BANK1 321.[8] Audio signals are sampled at a sampling rate of 48 KHz. During each sampling period, 16 samples from 16 audio channels are received from the serial AES input ports and stored in the DRAM banks in recording mode. During the same sample period, the playback of the digital audio is done by reading the data stored in the DRAM banks and sending it to the serial AES output ports. [9]

---

[1] See specification, page 5, lines 17-24; page 7, lines 1-25; page 7, lines 20-25; page 8, lines 1-6.
[2] See specification, page 8, lines 19-20.
[3] See specification, page 8, lines 21-23; page 9, lines 1-2.
[4] See specification, page 9, lines 1-3; Figure 3.
[5] See specification, page 9, lines 5-7; Figure 3.
[6] See specification, page 9, lines 12-16.
[7] See specification, page 9, lines 17-21.
[8] See specification, page 9, lines 22-25.
[9] See specification, page 10, lines 4-10; Figure 4.

The audio samples are allocated in the memory banks such that the storage of all audio channels is distributed equally over the entire memory banks. For two memory banks, DRAM BANK0 is configured to store audio sampled data from the even channels and DRAM BANK1 is configured to store audio sampled data from the odd channels. This allocation scheme can be extended to more than two memory banks. [10] With this equal allocation, there is less chance for the SCSI controller and the DSP to access to the same memory bank at the same time. Even when they do, one processor does not have to wait for too long for its turn to access memory. The result is that audio sampled data are written into or read out of the memory banks at a fast rate to accommodate real-time processing.[11]

VI. ISSUES

The issues are:

(i) whether Claims 1-9 are unpatentable under 35 U.S.C. §103 in view of U.S. Patent No. 5,625,570, issued to Vizireanu et al. ("Vizireanu").

(ii) whether Claims 10-15 are unpatentable under 35 U.S.C. §103 over Vizireanu in view of U.S Patent No. 5,273,050 issued to Schaus et al. ("Schaus").

VII. GROUPING OF CLAIMS

Applicants contend that the claims of the present invention stand or fall together. In other words, claims 1-4, 10-13, and 5-9, 14-15 form a single group.

[10] See specification, page 10, lines 19-25; page 11, lines 1-2.
[11] See specification, page 11, lines 2-7.

VIII. ARGUMENTS

A. Claims 1-9 Are Unobvious over Vizireanu

Claims 1-9 were rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,625,570 issued to Vizireanu et al. ("Vizireanu"). Applicants respectfully traverse the rejection for the following reasons.

Vizireanu discloses a system for inserting individualized audio segments into prerecorded video media. Audio segments are simultaneously inserted into respective video tapes (Vizireanu, Col. 12, lines 3-4). Upon completion of the simultaneous insertion, the VTR is put in stop mode and the VTR units are signaled to eject (Vizireanu, Col. 16, lines 23-35).

Vizireanu does not disclose, suggest, or render obvious: (1) a plurality of semiconductor memory banks accessible to first and second processors for read and write operations; and (2) storing subsets of audio data corresponding to different groups of audio channels.

First, Applicants contend that Vizireanu does not disclose first and second processors. In the Office Action dated December 1, 1999, the Examiner states that the element 340 in Vizireanu is a processor. However, the element 340 in Vizireanu (Figure 3) is merely a 6 channel audio server card interfacing between the processor 20 to the VCR's 310. The audio server card 340 only provides the audio signal lines to send the audio segments (Vizireanu, Col. 19, lines 40-44). The definition of the word "processor" must be taken within the context of the specification. "The specification can always be used as a dictionary to learn the meaning of a term in the patent claim." *In re Boylan*, 392 F.2d 1017, 157 USPQ 370 (CCPA 1968). MPEP 804 II.B.1 "Further, those portions of the

specification which provide support for the patent claims may also be examined and considered when addressing the issue of whether a claim in the application defines an obvious variation of an invention claimed in the patent." *In re Vogel*, 422 F.2d 438, 441-42, 164 USPQ 619, 622 (CCPA 1970). MPEP 804 II.B.1. Here, the word "processor" is used in the claim with full support from the specification to refer to a "microprocessor" or "digital signal processor". See Specification, page 7 (lines 3-5) and page 8 (lines 1-3, lines 14-15, lines 18-20). As well known, a microprocessor or a digital signal processor is a device that can execute instructions in a program. The audio server card 340 in Vizireanu cannot operate as a microprocessor or a digital signal processor. Nowhere in Vizireanu that a description of the audio server card 340 functioning as a microprocessor is found. In fact, the audio server card 340 cannot be a microprocessor because Vizireanu clearly shows that the four audio server cards 340 are connected to a computer 320.

Second, Applicants contend that Vizireanu does not disclose a plurality of memory banks. In the Office Action dated December 1, 1999, the Examiner stated that the VCR 310 is read as a memory bank because "the function of the VCR is to store data (write) and to retrieve data (read) when being accessed." (Office Action, page 5). Applicants respectfully disagree with this overly broad interpretation of a memory bank. As is well known by the public, a VCR is a mechanical device with magnetic tape that can record audio segments. A VCR is not a memory bank. In the present invention, the memory banks include semiconductor memory devices, as opposed to magnetic tape. In the Office Action dated November 20, 2000, the Examiner states that "it would have been obvious to one of ordinary skilled in the art at the time the invention was made to equivalently substitute the memory banks of Vizireanu with any well known semiconductor memory devices..." However, the VCR device cannot be equivalently substituted by the memory banks because a VCR device is a mechanical device with interface structure totally

different from semiconductor devices. Furthermore, VCR devices are not suitable for realtime audio processing from a plurality of audio channels.

Third, Vizireanu does not disclose, suggest, or render obvious storing subsets of audio data corresponding to different groups of audio channels. Vizireanu merely teaches audio segments are simultaneously inserted into respective video tapes (Vizireanu, Col. 12, lines 3-4).

For these reasons, Applicants contend that independent Claims 1 and 5, and their respective dependent claims are distinguishable over Vizireanu.

B. Claims 10-15 Are Unobvious over Vizireanu in view of Schaus

Schaus discloses an electrocardiographic (ECG) system with multiple cassette loader. The multiple cassette loader is used to insert tapes into cassette player and to retrieve and restack ejected tapes from cassette player after they have been read (Schaus, Col. 3, lines 27-30).

As discussed above, Vizireanu and Schaus, take alone or in combination, do not disclose, suggest, or render obvious: (1) a plurality of semiconductor memory banks accessible to first and second processors for read and write operations; and (2) storing subsets of audio data corresponding to different groups of audio channels.

In the Office Action dated December 1, 1999, the Examiner stated that Schaus teaches that the data are stored and retrieved in a ping-pong operation. However, a ping-pong operation is not the same as interleaving the subsets of data.

In summary, Vizireanu and Schaus, take alone or in combination, do not disclose, suggest, or render obvious: (1) a plurality of semiconductor memory banks accessible to first and second processors for read and write operations; and (2) storing subsets of audio

data corresponding to different groups of audio channels. In addition, "[t]o support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

In the present invention, the cited references do not expressly or implicitly suggest: (1) a plurality of semiconductor memory banks accessible to first and second processors for read and write operations; and (2) storing subsets of audio data corresponding to different groups of audio channels.

C. Conclusion

The Federal Circuit stated that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. In re Vaeck, 947 F.2d. 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Furthermore, M.P.E.P. § 2142 states that:

> "To establish a prima facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Neither one of Vizireanu and Schaus discloses, suggest, or render obvious: (1) a plurality of semiconductor memory banks accessible to first and second processors for read and write operations; and (2) storing subsets of audio data corresponding to different groups of audio channels.

As a result, none of the cited references discloses, suggests, or renders obvious the present invention as recited in Claims 1-9 and 10-15.

Applicants respectfully request that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated or rendered obvious by the prior art.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: May 15, 2001

THINH V. NGUYEN
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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (Twice Amended) A method for allocating real-time audio data from a first plurality of audio channels in a system having a first processor and a second processor, the method comprising:

providing a second plurality of memory banks of semiconductor memory devices, each memory bank being accessible to the first and second processors for operations selected from the group comprising read and write operations; and

storing subsets of said audio data in the second plurality of memory banks, the subsets corresponding to different groups of audio channels.

2. (Amended) The method of claim 1, further comprising selecting said memory banks for access by one of the first and second processors.

3. (Amended) The method of claim 1 wherein the second plurality of memory banks includes two memory banks.

4. The method of claim 3 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

5. (Twice Amended) A system having first and second buses for processing real-time audio data from a first plurality of audio channels, the system comprising:

a first processor and a second processor coupled to said first and second busses, respectively; and

a second plurality of memory banks of semiconductor memory devices coupled to said first and second buses for storing said audio data, said second plurality of memory banks being accessible to the first and second processors for operations selected from the group comprising read and write operations, said second plurality of memory banks storing subsets of audio data, said subsets corresponding to different groups of audio channels.

6. (Amended) The system of claim 5 further comprises a plurality of selectors coupled said first and second buses to select said memory banks for access by one of said first and second processors.

7. (Amended) The system of claim 6 wherein the plurality of selectors include a plurality of address multiplexers and data transceivers.

8. The system of claim 5 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

9. (Amended) The system of claims 5, wherein the memory banks include dynamic random access memories.

10. The method of claim 1, wherein storing further comprises interleaving the subsets of data.

11. The system as set forth in claim 5, wherein the subsets are stored in the memory banks in an interleaving manner.

12. The method of claim 1, wherein storing comprises storing one of the subsets of audio data in one of the memory banks, said method further comprising reading stored audio data from a second of the memory banks.

13. The method as set forth in claim 1, wherein the first processor performs a read operation on a first memory bank of the plurality of memory banks and the second processor performs a write operation on a second memory bank of the plurality of memory banks.

14. The system of claim 5, wherein subsets of audio data are stored in one of the memory banks and stored audio data is read from a second of the memory banks.

15. The system as set forth in claim 5, wherein the first processor performs a read operation on a first memory bank of the plurality of memory banks and the second processor performs a write operation on a second memory bank of the plurality of memory banks.